In the Claims:

Please withdraw claims 9-21. Please amend claims 1 and 2. Please add new claims 22-25. Claims 1-4, 7, 8 and 22-25 are currently pending based on the amendment herein:

Claim 1. (Currently Amended) A semiconductor device comprising:

a substrate;

at least one fuse embedded within an interior portion of the substrate;

a continuous etch resistant layer on an exterior surface of the substrate, wherein the etch resistant layer is directly over an entire surface of the at least one fuse, and wherein the etch resistant layer is in direct mechanical contact with the at least one fuse; and

at least one insulative layer directly above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove.

Claim 2. (Currently Amended) The semiconductor device of claim 1, further comprising an alignment mark formed on the substrate at a location spatially removed from the fuse, wherein the alignment mark is adapted to provide an optical target for a laser.

Claim 3. (Original) The semiconductor device of claim 2, wherein the alignment mark further comprises the etch resistant layer thereover.

Claim 4. (Original) The semiconductor device of claim 2, wherein the fuse and the alignment mark are formed within a metal wiring layer of the device.

Claims 5 and 6 (Canceled)

Claim 7. (Original) The semiconductor device of claim 1, wherein the etch resistant layer comprises silicon nitride.

Claim 8. (Original) The semiconductor device of claim 1, wherein the etch resistant layer has a thickness of approximately 10-100 nm.

9. (Withdrawn) A method of forming a fuse structure, comprising:

providing a substrate having at least one fuse formed therein; and

depositing an etch resistant layer over a surface of the substrate.

10. (Withdrawn) The method of claim 9, further comprising providing an alignment mark formed within the substrate at a location spatially removed from the fuse.

11. (Withdrawn) The method of claim 9, wherein the etch resistant layer comprises silicon nitride.

12. (Withdrawn) A method of performing a fuse deletion process, comprising:

providing a substrate having at least one fuse therein, an etch resistant layer over the fuse and at least one insulative layer over the etch resistant layer;

removing a portion of the at least one insulative layer above the fuse to the etch resistant

layer; and

applying a radiant energy source to the fuse until the etch resistant layer is partially removed.

13. (Withdrawn) The method of claim 12, further comprising providing an alignment mark formed within the substrate having the etch resistant layer and at least one insulative layer thereover.

14. (Withdrawn) The method of claim 13, wherein the fuse and the alignment mark are formed within a metal wiring layer of the substrate.

15. (Withdrawn) The method of claim 13, further comprising removing a portion of the at least one insulative layer above an electrical feature and the alignment mark while removing the at least one portion of the at least one insulative layer above the fuse.

16. (Withdrawn) The method of claim 12, wherein removing a portion of the at least one insulative layer further comprises etching the insulative layer.

17. (Withdrawn) The method of claim 12, wherein applying a radiant energy source further comprises emitting a laser beam into the fuse.

18. (Withdrawn) The method of claim 13, further comprising:

locating the alignment mark with the radiant energy source; and

locating the fuse based upon the location of the alignment mark.

19. (Withdrawn) The method of claim 13, wherein the etch resistant layer provides a uniform passivation thickness over the fuse and the alignment mark.

20. (Withdrawn) The method of claim 12, wherein the etch resistant layer comprises silicon nitride.

21. (Withdrawn) The method of claim 19, wherein the etch resistant layer has a thickness of approximately 10-100 nm.

Claim 22. (New) The semiconductor device of claim 1, wherein the substrate comprises at least one metal wiring layer within the substrate, and wherein a first region of the metal wiring layer comprises the fuse.

Claim 23. (New) The semiconductor device of claim 22, wherein a plurality of remaining regions of the metal wiring layer are electrically connected to contact pads.

Claim 24 (New) The semiconductor device of claim 1, wherein the exterior surface of the substrate is coplanar with the entire surface of the at least one fuse.

Claim 25 (New) The semiconductor device of claim 2, wherein the substrate comprises at least one metal wiring layer within the substrate, wherein a first region of the metal wiring layer comprises the fuse, and wherein a second region of the metal wiring layer comprises the alignment mark.